# Wafer-Level-System-Integration (WLSI) Technologies for 2D and 3D System-in-Package

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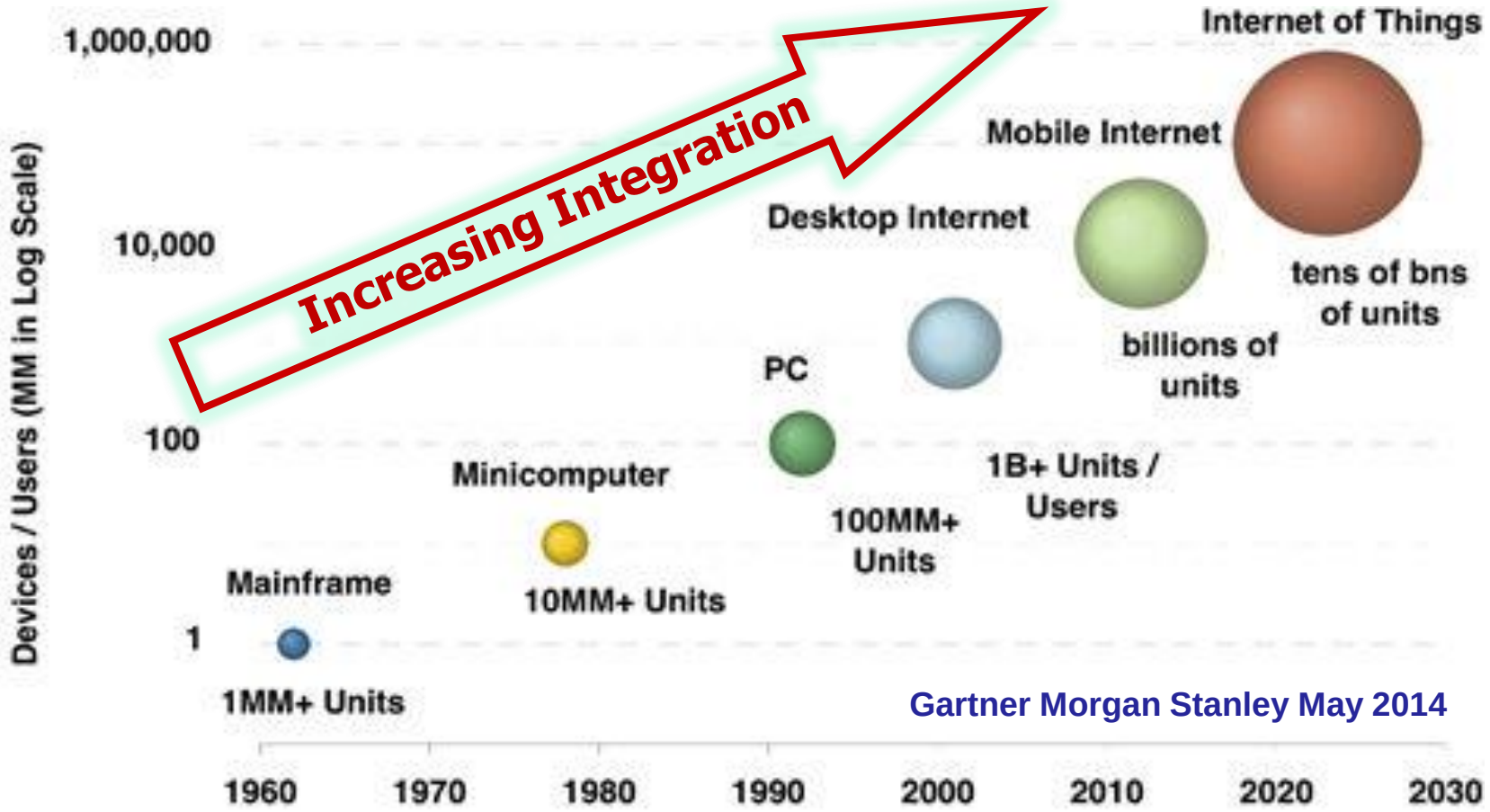
**TSMC R&D**

# Outline

- Motivation-
  - Industry trends
- New SiP Technologies
  - CoWoS Integration
  - Integrated Fan-Out WLP (InFO)
- Conclusions and Outlook

# Trend and Motivation






Gartner Morgan Stanley May 2014

# Semiconductor Product Revolutions



| DT/NB PC | Smart Mobile | IoT/IoE |
|---|---|---|
|  |  |  |
| *Fast, faster, faster* | *Cost, power, form-factor* | *Lower and smaller* |
| *More Moore* | *More & More-than Moore* | *More-than Moore* |
| *High Performance* | *Optimized for User Exp'ce* | *Wide-spectrum Systems* |

# Semiconductor Market Trend



- **Smart Mobile and IoT/IoE**
  - System and modular devices
  - Lower cost, faster cycle-time and TTM
  - Light, thin, small, cool, green, fashionable
- **High Performance (Clouds)**
  - Power, memory bandwidth, data rate
  - Cost competitive
- **Moore's Law Challenges**
  - More challenging to maintain scaling factor (density) and cost against schedule.
  - Good SiP technologies create values and reduce Moore's Law pressure.

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  - **CoWoS Integration**
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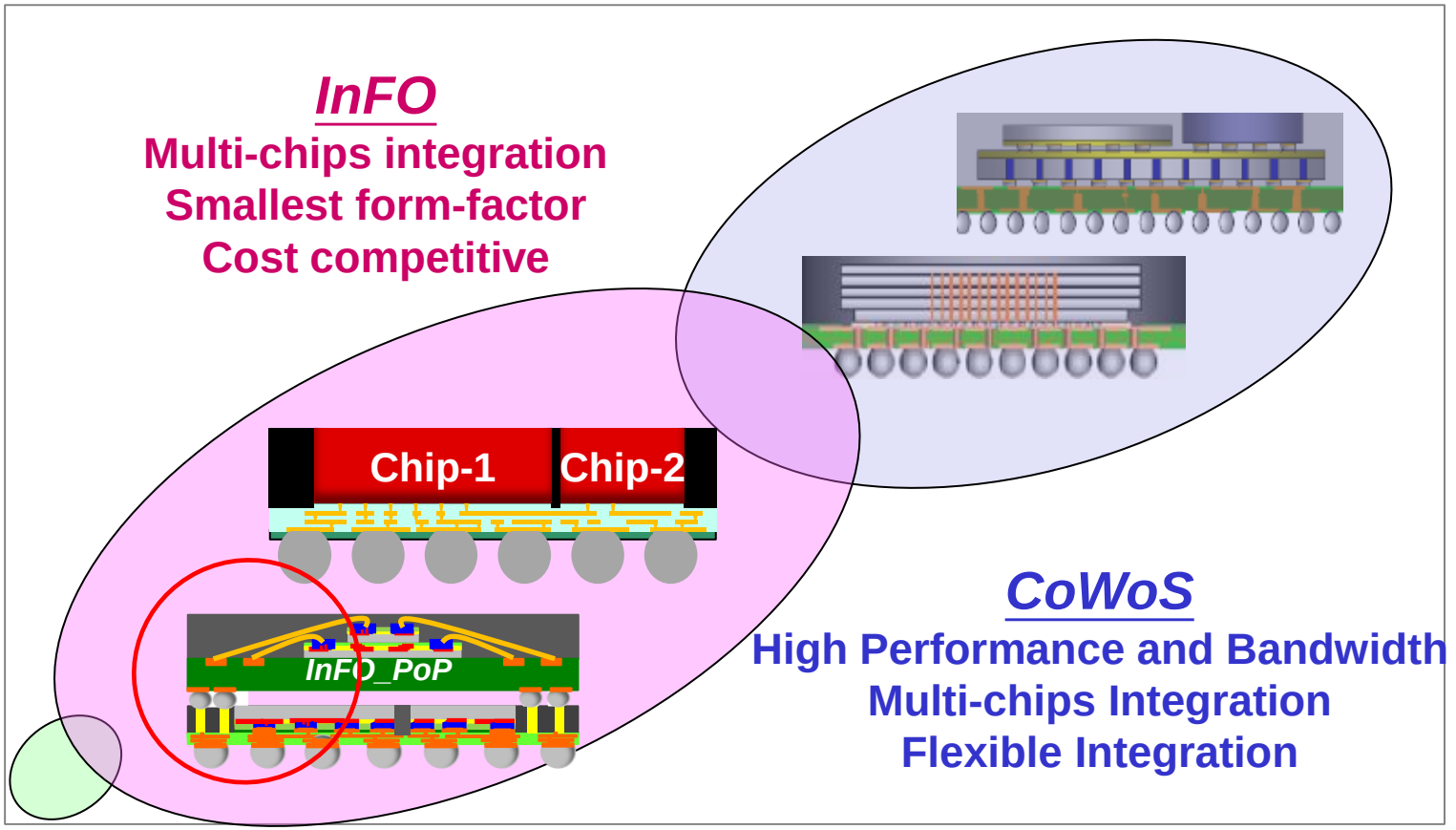
# TSMC WLSI Technologies

## Full spectrum applications




I/O to Substrate and/or PCB

WLCSP

TSV (3D-IC) & TIV (InFO_PoP)

Die/PKG size ($mm^2$)

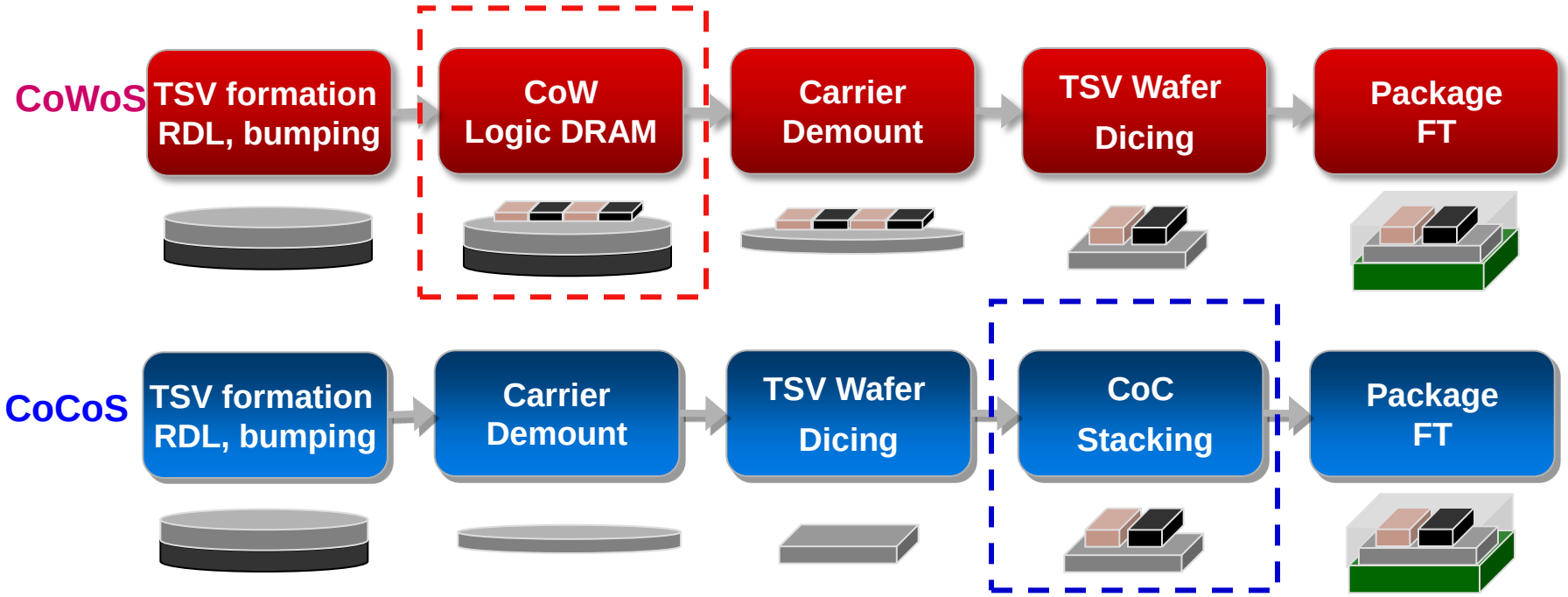
# TSMC WLSI Technologies



- **WLSI Technologies**
  - Innovative Adv. PKG technologies in “wafer form”
  - Leverage TSMC core competence and Grand Alliance
  - Full spectrum- 2D→3D, Mobile→HP, and Today→NBTs.
- **Enable Chip-Partition**
  - Sustain Moore’s Law longer. Re-use technology/capacity and Design/IP (Adv./Mature, Analog/Digital, Logic/DRAM…)
  - Built-in high-Q inductor on both Fan-In and Fan-Out WLP with chip cost savings. Enable Active/passive partition.
- ***Powerful*** **and** ***Cool*** **Integration**
  - Integrate Chips (advanced, specialty) and PKGs
  - PKG/Chip backside exposed, better thermal perform.
  - Total Solution with single Design PDK, CT and TTM adv..

# CoWoS™ Integration Flow



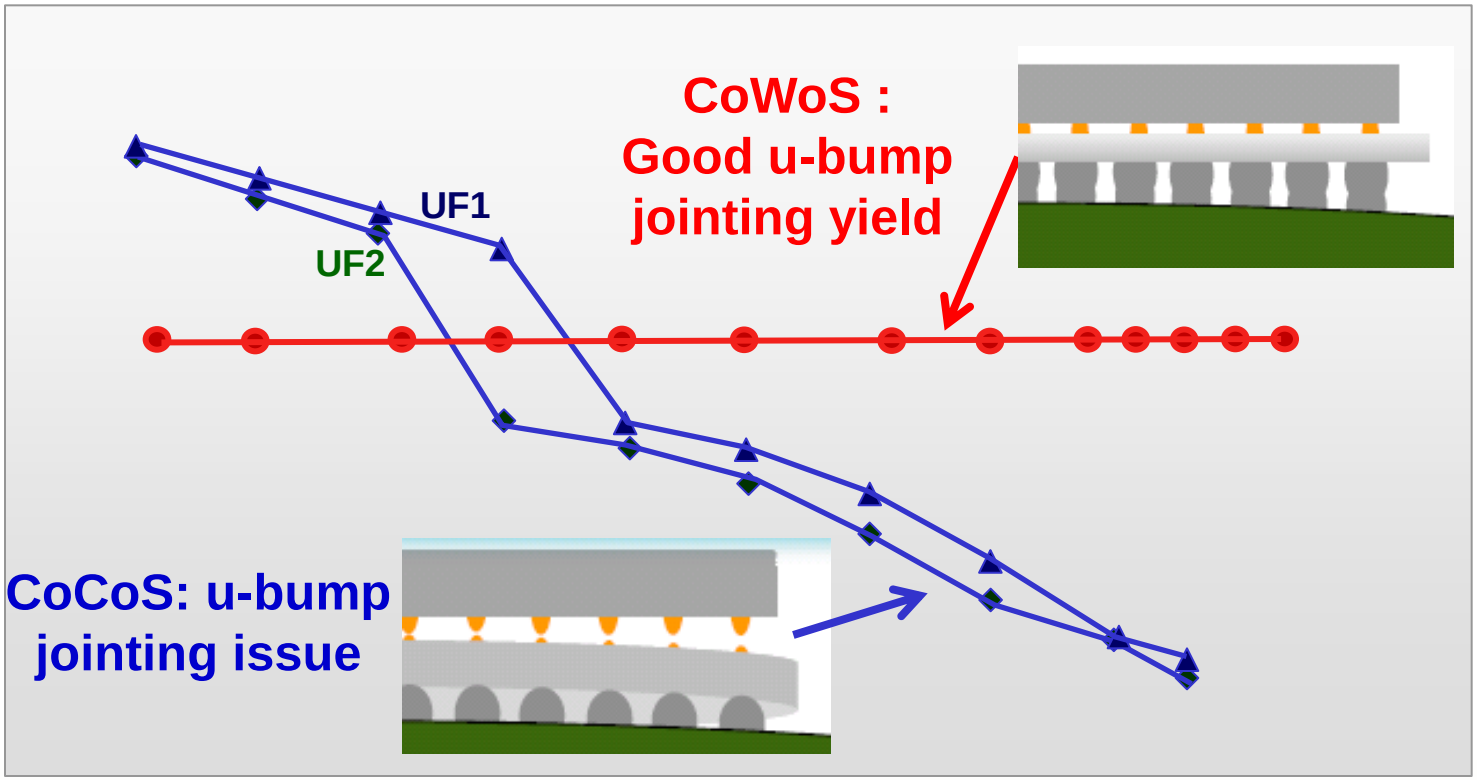



- CoWoS™ is a better integration and stacking flow on thin wafer/chips.
- Flexible integration of multi-chips for both Interposer and 3DIC.
- Low demanding substrate (embedded chips, cost, warpage control, and layers, etc) than other approaches, with yield and reliability advantages

# CoWoS- Superior Warpage Control Enabling Excellent Yield

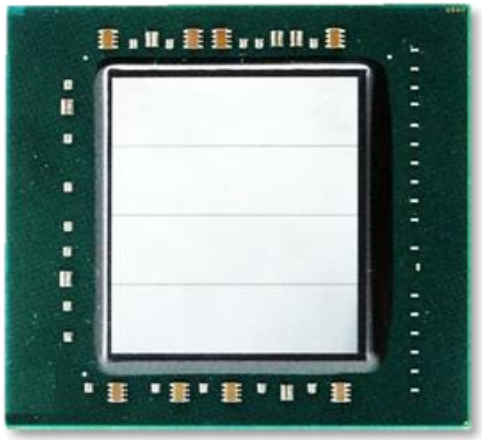


**Thin 3D Die warpage > μ-bump height**
**→ Poor joint yield**



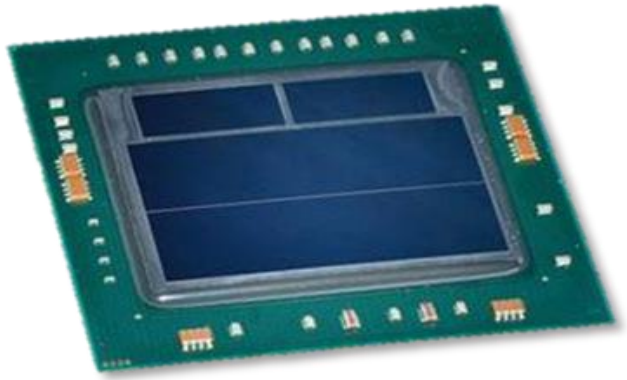
# Commercialization of CoWoS™ Interposer Stacking

Courtesy of Xilinx



Homogeneous

Courtesy of Xilinx

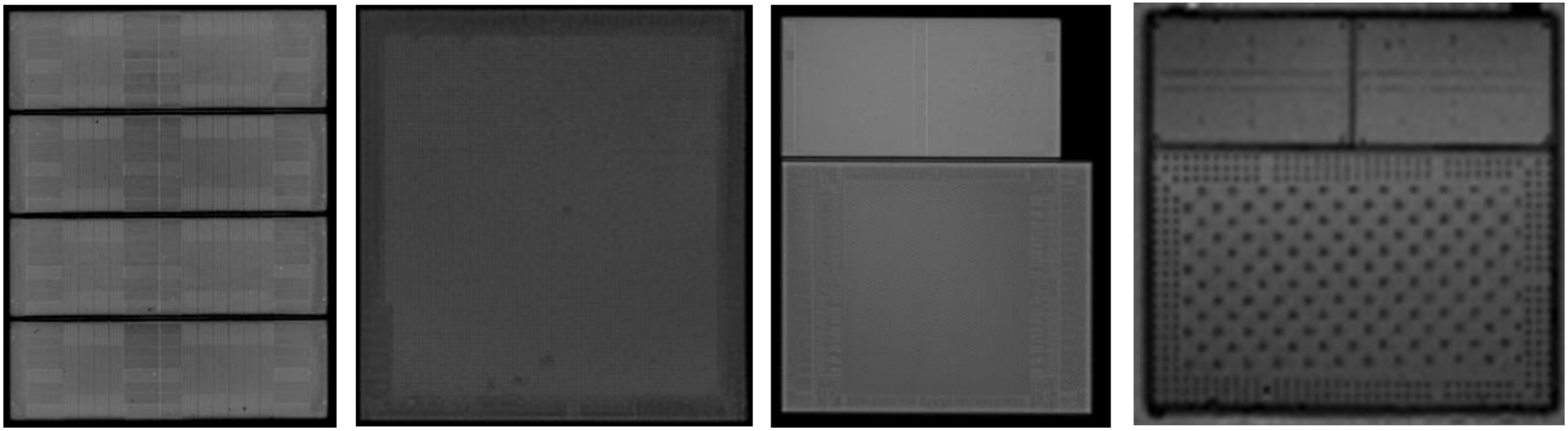


Heterogeneous

**Both integrations use CoWoS™ integration flow.**

# CoWoS™ Implementation of Flexible Multi-Chips Layouts



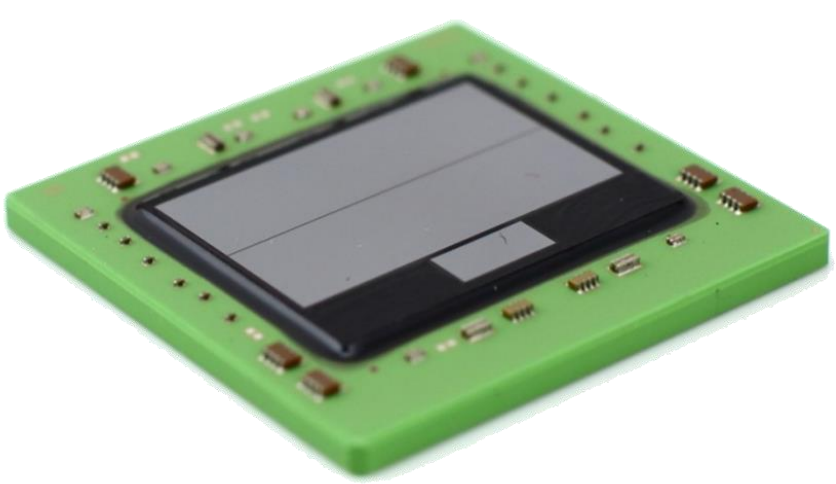


- High flexibility/efficiency chip layouts.
- Maximum integrity with single piece Si interposer and single (μ)-bump pitch- *yield* and *reliability* advantages.
- "Single" assembly (vs. multiple bridges / assemblies) on *simplified substrate* (vs. embedded substrate).

# CoWoS™ Enable High Performance

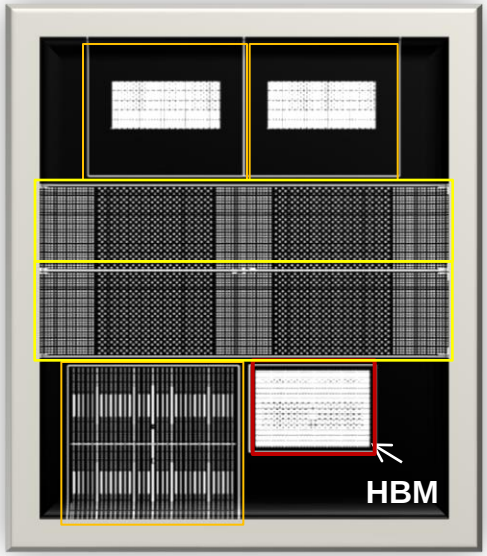


- Chip-partition into same or different nodes with ultra-high interconnect density
- Integrate WIO or HBM with Logics, exceeding full reticle size.



(Pictures Courtesy of Xilinx)

***Floor Plan***

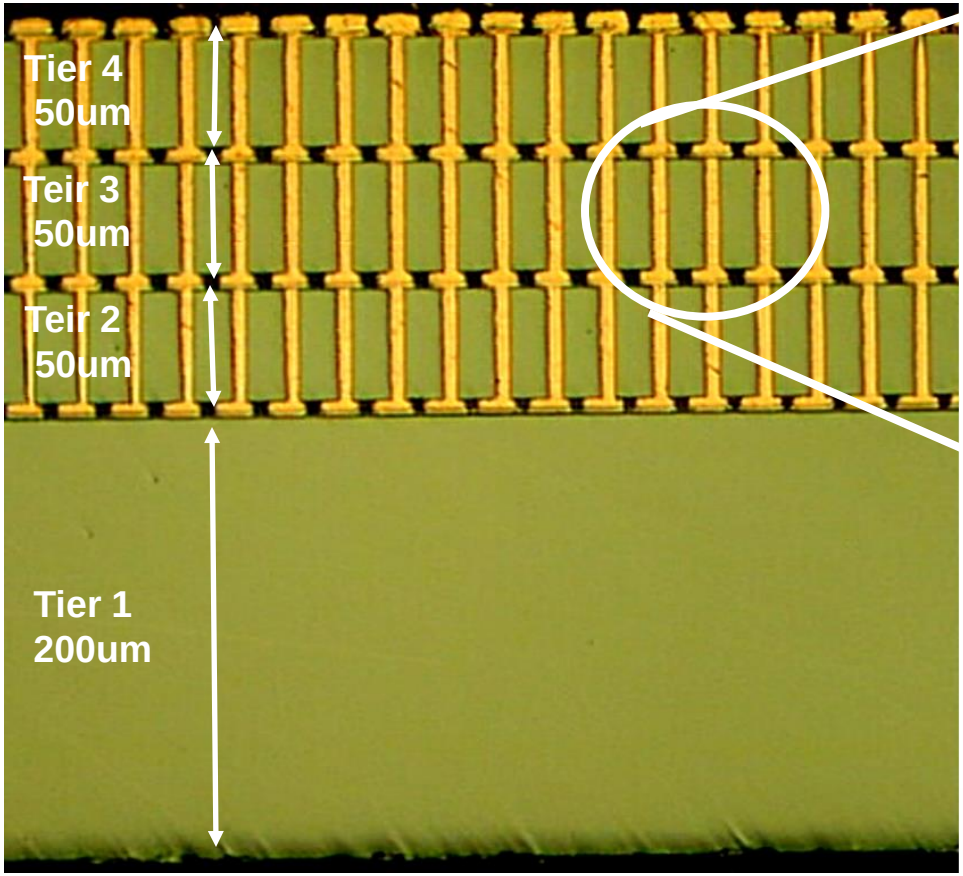


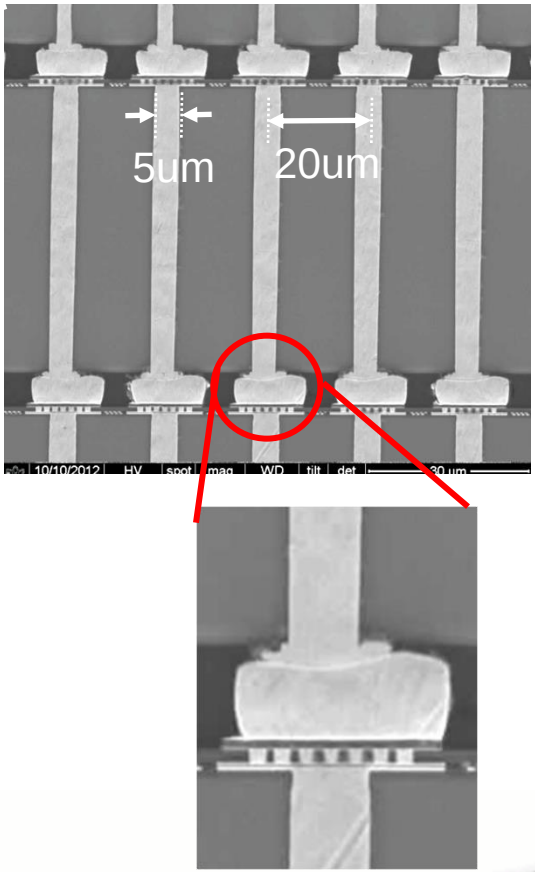

**HBM: High bandwidth memory**

# Multi-Tier TSV Scaling for 3D-IC



- Low-cost, high-density bond.
- Multi-tier stacking demonstrated.

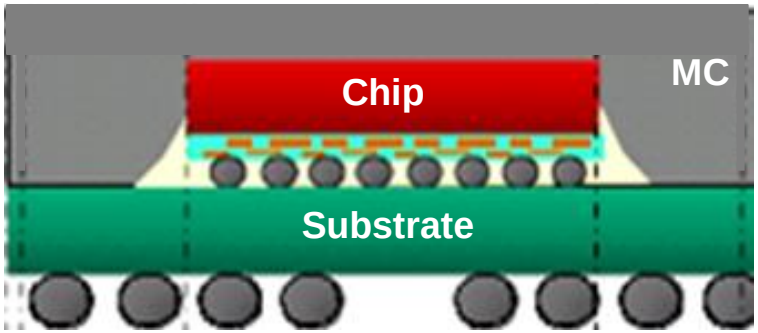


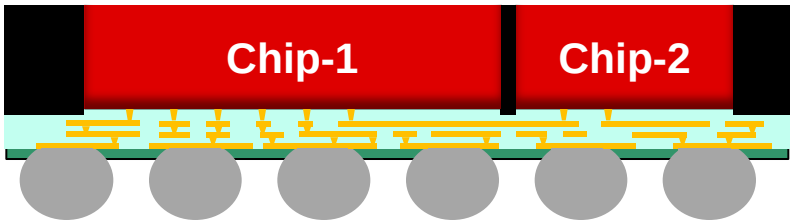
# Values from Subtraction



**Flip Chip**



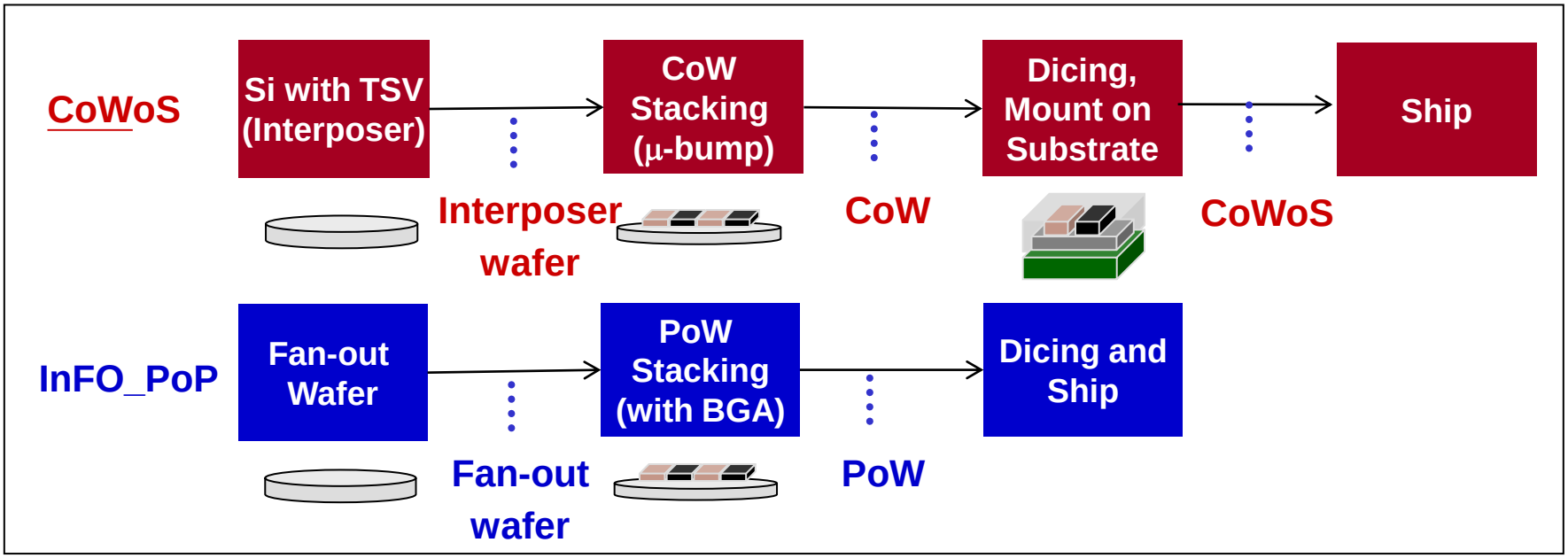

**InFO-WLP**




- **Flip-Chip**
  - Substrate and bump add to total thickness and $R_{th}$
  - Bumping and assembly cost
- **Integrated Fan-Out WLP (InFO)**
  - Simplified architecture.
  - Lower profile, cost and $R_{th}$.
  - Powerful and Cool integration: single- and multi-chips, 2D/3D, Mobile/HP, Today/NBTs, and Logic/memory, Adv./Mature nodes Logics, etc.

# InFO_PoP Leverages CoWoS



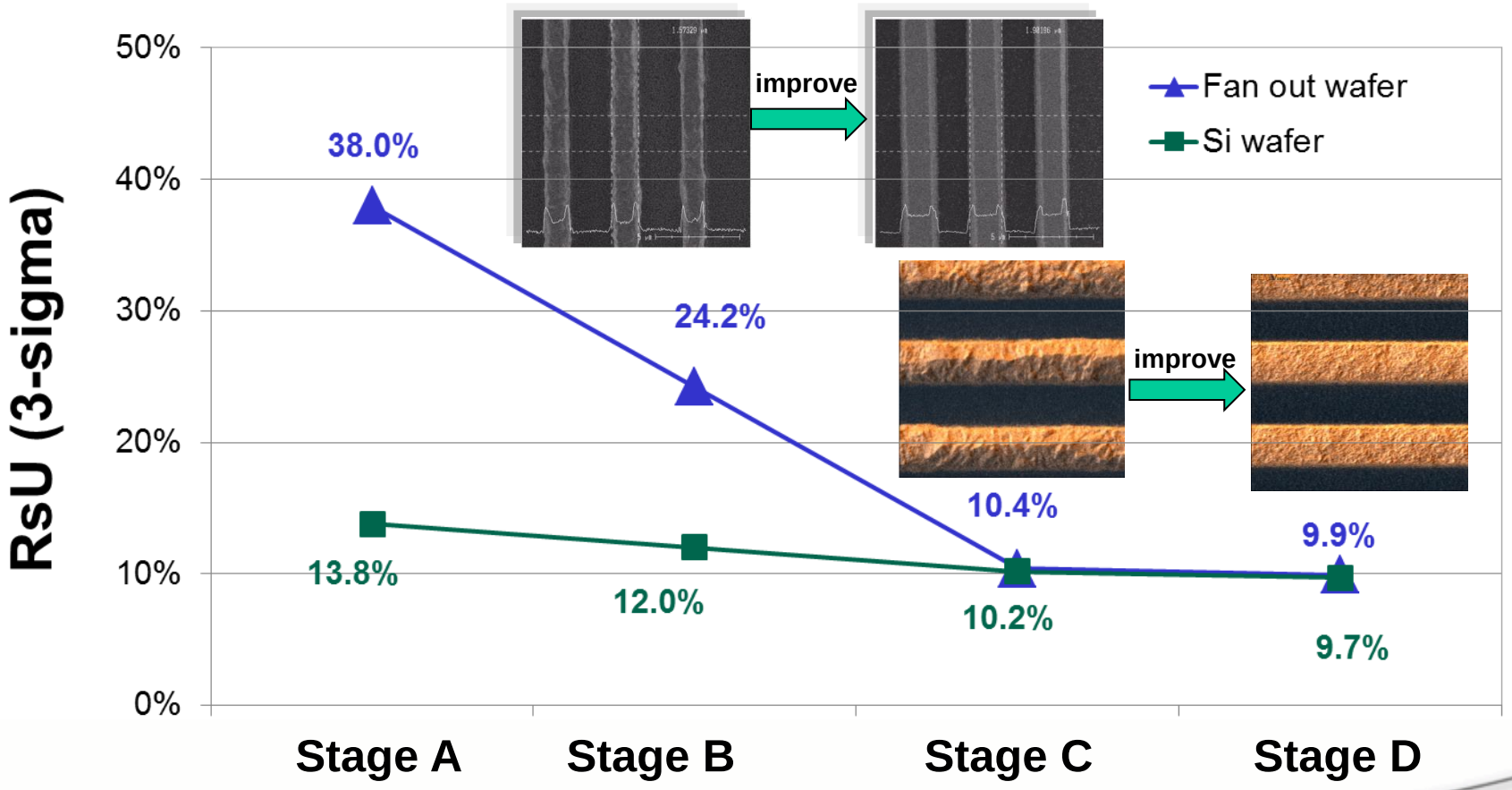



- CoWoS: SoC Chips stack on TSV wafer.
- InFO_PoP: PoW (PKG-on-Wafer) DRAM PKG stack on InFO wafer. Key processes sharing: Thin wafer process, Carrier bond/de-bond, and RDL, etc.

# InFO RDL Tight Process Control



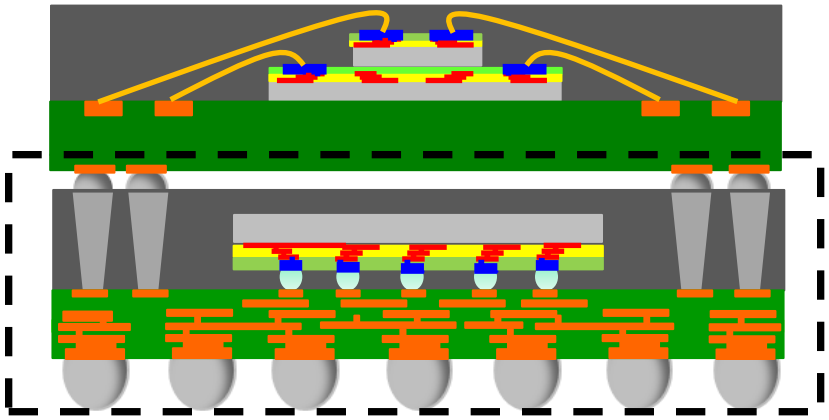
- **W/S=2/2μm, Rs variation (RsU) 3σ ≤ 10%**

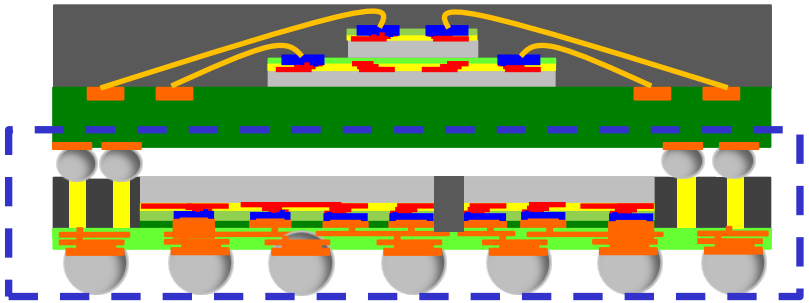


# TSMC InFO_PoP for AP/DRAM System-Integration



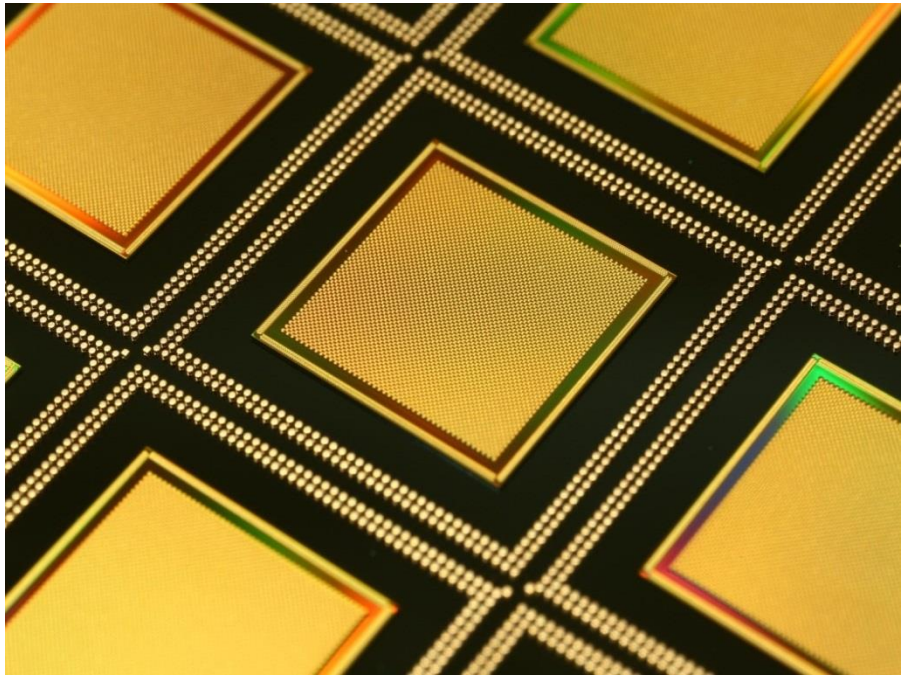
- Integrated Fan-Out WLP (InFO) grows from 2D InFO to 3D InFO_PoP (MoL Stacking).
- Leadership in low profile, low power, high memory bandwidth with competitive cost



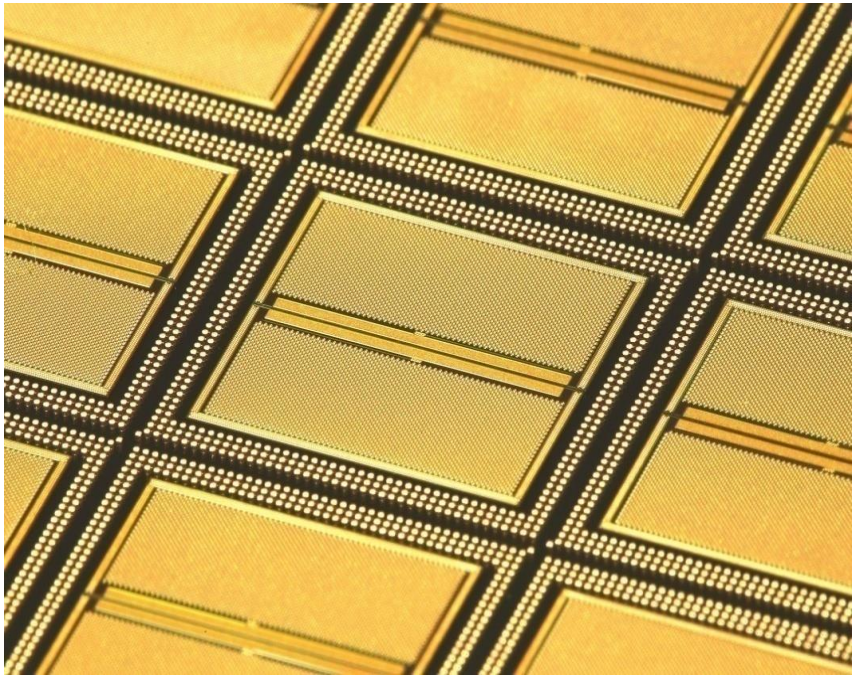


# TSMC InFO_PoP with TIV - Top View

- Wafer form process, capable of very high density TIV Integration for high bandwidth.



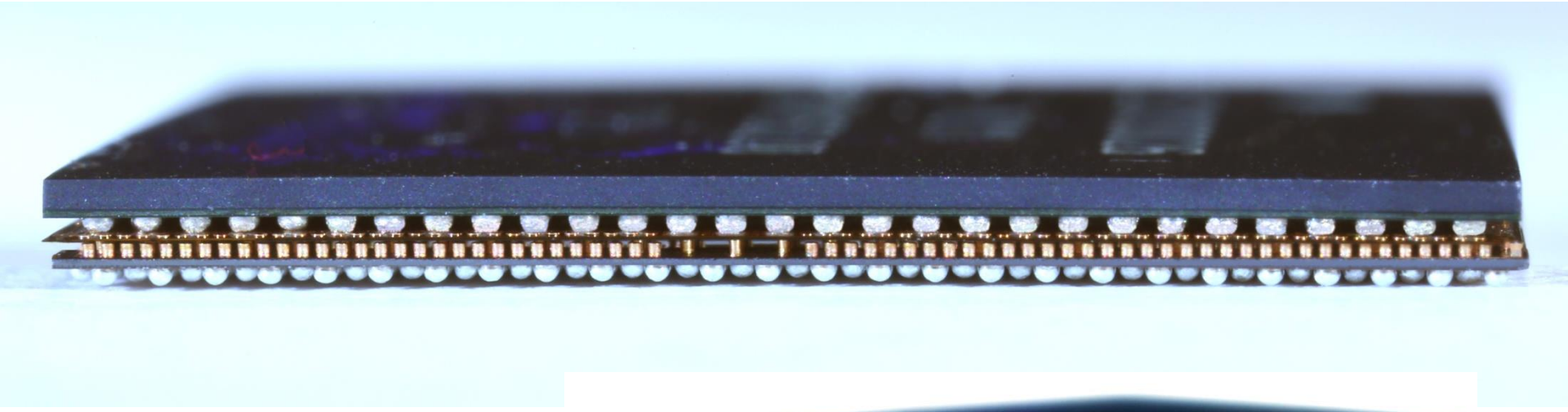
Single-Chip InFO_PoP



Dual-Chip InFO_PoP

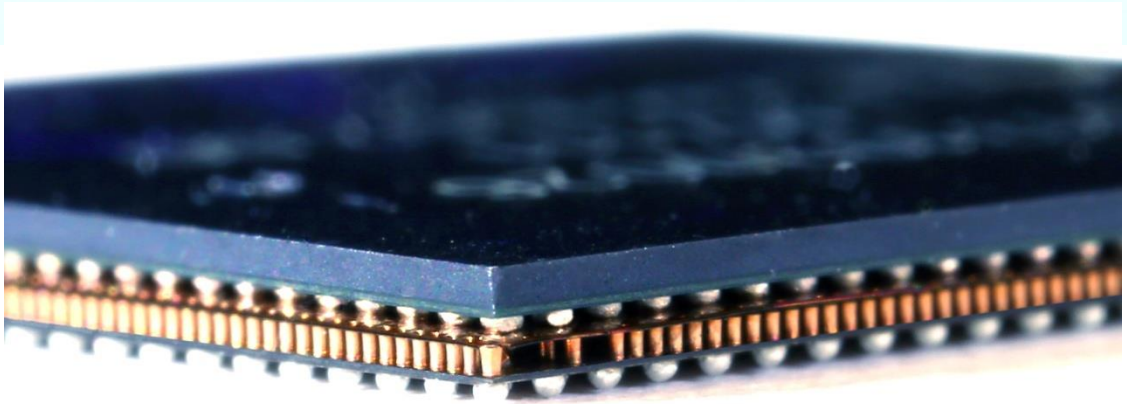
# TSMC InFO-PoP
# 3D-Stacking with DRAM PKG





DRAM →

InFO with TIV →



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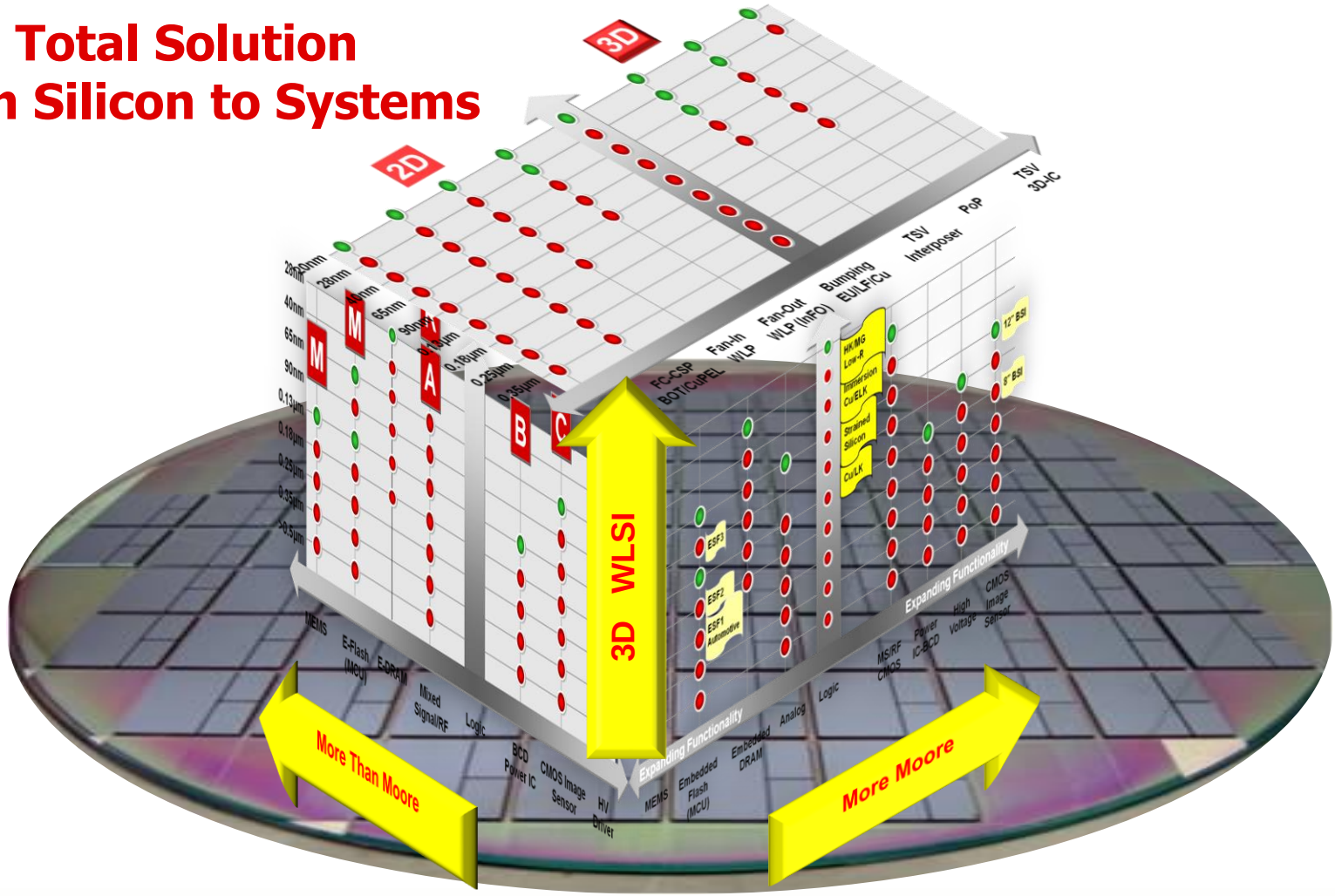
# Most Powerful System Integration



## Total Solution
## From Silicon to Systems




## Wafer Level System Integration
## WLSI

# Summary

- TSMC WLSI Technologies developed for wide-range applications- 2D/3D, Mobile/HP, and Today/NBTs.
- Total Solution from Silicon to System with innovative, disruptive and cost-competitive Adv. PKG options. Paradigm shift from IC- to System-Foundry.
- Enable Chip-Partition, Powerful and Cool Integration. Sustain Moore's Law longer.